I. Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Currently Amended) ~~The method of claim 1, said creating an inductor in or adjacent to the surface of a layer of dielectric overlying the surface of said substrate~~ A method for the creation of a suspended inductor, comprising the steps of:

providing a substrate;

~~creating a layer of pad oxide over the surface of said substrate;~~

depositing a layer of dielectric over the surface of said substrate ~~layer of pad oxide~~;

depositing a layer of etch stop material over the surface of said layer of dielectric;

patterning and etching said layer of etch stop material, thereby creating a pattern of said inductor through the layer of etch stop material;

etching said layer of dielectric to a measurable depth in accordance with said pattern created through said layer of etch stop material, creating a pattern for said inductor in said layer of dielectric; ~~and~~

filling said pattern created in said layer of dielectric with an inductor material to a measurable height[[.]];

exposing the surface area of said layer of dielectric; and

etching the exposed surface area of said layer of dielectric, thereby creating an air gap in said layer of dielectric, said air gap surrounding said inductor material.

3. (Original) The method of claim 2, said exposing surface areas of said layer of dielectric further comprising additional steps of:

removing said patterned and etched layer of etch stop material from the surface of said layer of dielectric where said layer of etch stop material aligns with said inductor and overlies a first plane formed by said first upper line of said first cross section of said spirals of said inductor, said first plane further being parallel with the surface of said substrate; and

removing said layer of dielectric where said layer of dielectric aligns with said inductor and overlies said first plane.

4. (Currently Amended) The method of claim 2, additionally comprising a step of creating at least one supporting pillar for said inductor through said layer of dielectric, said additional step being

performed prior to said filling said pattern created in said layer of dielectric with ~~a metal~~ an inductor material to a measurable height.

5. (Currently Amended) The method of claim 2 [[1]], said etching the exposed surface areas of said layer of dielectric comprising exposing said exposed surface areas of dielectric to an etchant, ~~having high etch sensitivity for said layer of dielectric~~ said etchant having a ratio between a rate of removal of said layer of dielectric and a rate of removal of said inductor material, thereby removing said exposed layer of dielectric by a measurable amount.

6. (Currently Amended) The method of claim 5, said etchant ~~comprising~~ configured to create sidewalls with slope in the dielectric.

7. (Canceled)

8. (Currently Amended) The method of claim ~~7~~ 5,, said ~~slope etcher~~ etchant being used under conditions of applying, per liter of slope and contained therein: 107 ml of DIW, 509 ml of BOE diluted in the ratio of 10:1, 35 ml of 49% HF and 349 ml of CH_3OOH [[CH_3OH]], applied at a temperature of 25 degrees C. and for the time of 1 minute.

9. (Original) The method of claim 4, said step of creating at least one supporting pillar comprising steps of creating patterned and etched overlying layers of semiconductor material, said patterned and etched overlying layers of semiconductor material underlying and being aligned with at least one element of said pattern of said inductor, said patterned and etched overlying layers of semiconductor material having an etch sensitivity when applying a first etchant thereto that is lower than the etch sensitivity of said layer of dielectric when applying said first etchant thereto by a measurable amount.

10. (Currently Amended) The method of claim 2 [[1]], said layer of dielectric comprising silicon dioxide, created to a thickness not less than about 5.0 μm.

11. (Currently Amended) The method of claim 2 [[1]], said inductor being a spiral inductor.

12. (Original) The method of claim 2, said measurable height being about 1.2 μm.

13. (Currently Amended) The method of claim 9, said patterned and etched overlying layers of semiconductor material comprising material selected from the group consisting of polysilicon, ~~and contact pad material and~~ silicon nitride, metals, and dielectrics.

14. (Original) The method of claim 4, said step of creating at least one supporting pillar comprising steps of creating patterned and etched overlying layers of semiconductor material, said patterned and etched overlying layers of semiconductor material underlying and being aligned with at least one element of said pattern of said inductor, said patterned and etched overlying layers of semiconductor material having an etch sensitivity that is less than an etch sensitivity of an oxide based layer of dielectric by a measurable amount.

15–26. (Canceled)

27. (Original) The method of claim 2, said layer of etch stop material comprising silicon nitride (Si_3N_4).

28–45. (Canceled)

46. (New) A method for the creation of a suspended inductor, comprising the steps of:

providing a substrate;

depositing a layer of dielectric over the surface of said substrate;

depositing a layer of etch stop material over the surface of said layer of dielectric;

creating a pattern of said inductor through the layer of etch stop material;

patterning said layer of dielectric in accordance with said pattern created through said layer of etch stop material, thereby creating a pattern for said inductor in said layer of dielectric;

filling said pattern created in said layer of dielectric with an inductor material; and

patterning said layer of dielectric, thereby creating an air gap in said layer of dielectric, said air gap surrounding said inductor material.

47. (New) The method of claim 46, said patterning said layer of dielectric further comprising additional steps of:

removing said patterned and etched layer of etch stop material from the surface of said layer of dielectric where said layer of etch stop material aligns with said inductor and overlies a first plane formed by said first upper line of said first cross section of said inductor, said first plane further being parallel with the surface of said substrate; and

removing said layer of dielectric where said layer of dielectric aligns with said inductor and overlies said first plane.

48. (New) The method of claim 46, additionally comprising a step of creating at least one supporting pillar for said inductor through said layer of dielectric, said additional step being performed prior to said filling said pattern created in said layer of dielectric with an inductor material.

49. (New) The method of claim 46, said patterning said layer of dielectric comprising exposing the surface area of said dielectric to an etchant, said etchant having a ratio between a rate of removal of said layer of dielectric and a rate of removal of said inductor material, thereby removing said layer of dielectric.

50. (New) The method of claim 48, said step of creating at least one supporting pillar comprising steps of creating patterned overlying layers of semiconductor material, said patterned overlying layers of semiconductor material underlying and being aligned with at least one element of said pattern of said inductor, said patterned overlying layers of semiconductor material having an etch sensitivity when applying a first etchant thereto that is lower than the etch sensitivity of said layer of dielectric when applying said first etchant thereto.